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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/029,649	12/20/2001	James C. McKinnell	10011490-1	5091

7590 08/18/2004

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EXAMINER	
MAI, ANH D	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 08/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/029,649	MCKINNELL, JAMES C.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-12,14-17,33 and 34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-12,14-17,33 and 34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of the Claims

1. Amendment filed July 21, 2004 has been entered. Claims 5, 13, 18-32 and 35-59 have been canceled. Claims 1, 10, 15 and 33 have been amended. Claims 1-4, 6-12, 14-17, 33 and 34 are pending.

Claim Objections

2. Claims 10-12 and 14 are objected to because of the following informalities:

Claim 10, line 8, recites: "the gold alloyed with **the oxide** is configured...".

The correct term should be: the gold alloyed with **the oxide affinity material** is configured...

Appropriate correction is required.

3. Claim 12 is further objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claim 12 recites: wherein the silicon layer on the first semiconductor wafer has a native oxide layer thereon.

The native oxide may be formed on the silicon layer before the bonding. However, when the wafers are bonded together, as claimed in claim 10, the native oxide has been reduced by the oxide affinity material.

Therefore, claim 12 does not further limit the scope of claim 10.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1, 3, 4, 6-10, 12, 14-16, 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Merchant et al. (U.S. Patent No. 6,118,181) of record, in view of Terasawa (U.S. Patent No. 5,702,962).

With respect to claim 1, Merchant teaches an electrical device substantially as claimed including:

first (21) and second (23) substrates, having first and second integrated circuits, respectively, wherein at least one of the first substrate or the second substrate has a semiconductor layer (31) thereon; and

a bond structure (33) bonding the first substrate (21) to the second substrate (23), the bond structure (33) including an alloy:

bonded to the semiconductor layer (31);

composed of noble metal (Pd); and

configured to form an electrical connection between the first integrated circuit and the second integrated circuit. (See Fig. 2E, col. 3-6).

Merchant also teaches: since palladium has experimentally been found to enable a lower bonding temperature, palladium is preferable to platinum, but in some embodiments, it may be possible to use platinum or other materials for the palladium. (See col. 4, lines 26-30).

Thus, Merchant is shown to teach all the features of the claim with the exception of using bonded structure composed of noble metal alloyed with an oxide affinity material.

However, Terasawa teaches a bond structure (62) composed of noble metal (Au) alloyed with an oxide affinity material (Sb) to electrically connecting two substrates (10 and 20) together. (See Fig. 2B, First Embodiment).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to alternatively bond the first and second substrates of Merchant using bonded structure composed of noble metal alloyed with oxide affinity material as taught by Terasawa because using such material (Au-Sb), the substrates can be bonded together at lower temperature, thus, warpage can be avoided.

With respect to oxide affinity material, Sb is a metal well known to have an affinity for oxygen higher than that of the material (Si) of which the semiconductor layer (10) is composed.

With respect to claim 3, the electrical device of Merchant further comprising electrical insulation (69) situated between the first (21) and second (23) substrates for electrically isolating a plurality integrated circuits. (See Fig. 2A).

With respect to claim 4, the electrical device of Merchant further comprising a region having a closed environment between the first (21) and second (23) substrates, wherein the region is defined at least in part by the bond structure (33).

With respect to claim 6, the bonding structure bonded to the semiconductor layer (31) of Merchant, in view of Terasawa, is sufficient to maintain an alignment of the first substrate (21) with respect to the second substrate (23).

With respect to claim 7, in view of Terasawa, the alloy (62, Au-Sb) bonded to the semiconductor layer (10) is composed of noble metal (Au) alloyed with an oxide affinity material (Sb), thus, having a free energy that is lower that that of silicon oxide.

With respect to claim 8, in view of Terasawa, the alloy (62, Au-Sb) bonded to the semiconductor layer (10) is composed of noble metal (Au) alloyed with an oxide affinity material (Sb), thus, more probable than not should have a free energy less than a range form about -200 Kcal/mol to about -205 Kcal/mol, as claimed.

With respect to claim 9, the alloy (62) of Terasawa bonded to the semiconductor layer (10) is composed of noble metal alloyed with a material selected from the group consisting of Sb.

With respect to claim **10**, Merchant teaches an electrical device substantially as claimed including: first (23) and second (21) semiconductor wafers including a plurality of integrated circuits, wherein:

the first semiconductor wafer (23) has a silicon layer (31) thereon;

the silicon layer (31) on the first semiconductor wafer (23) is bonded to the second semiconductor wafer (21) by a bonding structure; and

the bonding structure is configured to provide an electrical connection between at least one integrated circuit of the first semiconductor wafer (23) with at least one integrated circuit of the second semiconductor wafer (21). (See Figs. 2E, col. 3-6).

Merchant also teaches: since palladium has experimentally been found to enable a lower bonding temperature, palladium is preferable to platinum, but in some embodiments, it may be possible to use platinum or other materials for the palladium. (See col. 4, lines 26-30).

Thus, Merchant is shown to teach all the features of the claim with the exception of explicitly bonding the wafers using gold alloyed with an oxide affinity material.

However, Terasawa teaches bonding of first (23) and second (21) semiconductor wafers using gold alloyed with an oxide affinity material (Sb). (See Figs. 2B, First Embodiment).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to bond the semiconductor wafers of Merchant using gold alloyed with an oxide affinity material as taught by Terasawa because using such material (Au-Sb), the substrates can be bonded together at lower temperature, thus, warpage can be avoided.

With respect to the characteristics of Sb, Sb is well known in the art to have oxygen affinity higher than that of silicon.

With respect to claim 12, as best understood by the examiner, native oxide is known to form on the surface of silicon layer (31) prior to bonding.

With respect to claim 14, the electrical device of Merchant, in view of Terasawa, further comprising a hermetically sealed region between the first and second semiconductor wafers that is defined in part by:

the silicon layer on the first semiconductor wafer; and

the bonding structure, gold alloyed with the oxide affinity material.

With respect to claim **15**, Merchant teaches an electrical device substantially as claimed including:

first (23) and second (21) semiconductor wafers each including a plurality of integrated circuits;

silicon (31) on the first semiconductor wafer (23); and

a bonding structure (33) including noble metal, wherein the first semiconductor wafer (23) is bonded to the second semiconductor wafer (21) by the noble metal that is bonded to the silicon (31) on the first semiconductor wafer (23) such that the bonded structure is configured to provide an electrical connection between at least one integrated circuit of the first semiconductor wafer (23) with at least one integrated circuit of the second semiconductor wafer (21). (See Fig. 2B, col. 3-6).

Merchant also teaches: since palladium has experimentally been found to enable a lower bonding temperature, palladium is preferable to platinum, but in some embodiments, it may be possible to use platinum or other materials for the palladium. (See col. 4, lines 26-30).

Thus, Merchant is shown to teach all the features of the claim with the exception of explicitly formed a bond structure including gold alloyed with a material having a free energy lower than that of silicon oxide.

However, Terasawa teaches a bonded structure (62) includes gold alloyed with Sb to provide electrical connection between the first and second semiconductor wafer. (See Figs. 2B, First Embodiment).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to bond the semiconductor wafers of Merchant by a bonding structure including gold alloyed with Sb as taught by Terasawa because using such material (Au-Sb), the substrates can be bonded together at lower temperature, thus, warpage can be avoided.

With respect to the characteristics of Sb, Sb is well known in the art to have a free energy lower than that of silicon dioxide.

With respect to claim 16, the free energy of the Sb of Terasawa is well known to be less than a range from about -200 Kcal/mol to about -205 Kcal/mol as claimed.

With respect to claim **33**, Merchant teaches an electrical device substantially as claimed including:

first (21) and second (23) substrates bonded together with a first material (33);

the first material having is configured to form an electrical connection between a first integrated circuit on the first substrate (21) with a second integrated circuit on the second substrate (23). (See Fig. 2E, col. 3-6).

Merchant also teaches: since palladium has experimentally been found to enable a lower bonding temperature, palladium is preferable to platinum, but in some embodiments, it may be possible to use platinum or other materials for the palladium. (See col. 4, lines 26-30).

Thus, Merchant is shown to teach all the features of the claim with the exception of using the first material having dispersed therein a reducing agent for the diffusion therein of a second material of which at least one of the first and second substrates is composed.

However, Terasawa teaches a first (10 and second (20) substrates bonded together with a first material (62) having dispersed therein a reducing agent (Sb) for the diffusion therein of oxidation of second material (10) of which at least one of the first (10) and second (20) substrates is composed. (See Fig. 2B, First Embodiment).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to alternatively bond the first and second substrates of Merchant using the first material having dispersed therein a reducing agent as taught by Terasawa because using such material (Au-Sb), the substrates can be bonded together at lower temperature, thus, warpage can be avoided.

With respect to the characteristic of the reducing agent, Sb is a metal well known to have an affinity for oxygen higher than that of the Si, thus, Sb is more probable than not should be able to function as reducing agent for the diffusion of oxidation of the second material (Si) as well.

With respect to claim 34, in view of Terasawa, the first material (62) comprises gold and the second material (10) comprises silicon.

5. Claims 2, 11 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Merchant '181 and Terasawa '962 as applied to claim 15 above, and further in view of Ohara et al. (U.S. Patent No. 5,668,033) of record.

With respect to claims 2 and 11, Merchant and Terasawa teaches a bonding structure composed of noble metal, gold, alloyed with an oxide affinity material. It is well known that the lower bonding temperature is determined by the eutectic temperature of the noble metal and silicon.

Thus, Merchant and Terasawa are shown to teach all the features of the claim with the exception of explicitly disclosing the weight of the oxide affinity material in the noble metal alloy.

However, Ohara teaches the noble metal alloy is formed by significantly more Au then oxide affinity material, which is used to break Si-O bond so that good bondage between Au and Si can be achieved. (See col. 6, line 28-col. 9, line 6).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the bonding structure of Merchant and Terasawa, composed of noble metal alloyed with an oxide affinity material at an amount which is significantly less than the weight of noble metal, less than half, as taught by Ohara to form a bonding structure at lower temperature.

Note that, the higher amount of the oxide affinity material such as Ti, Pt, the higher the temperature of bonding, which lead to warpage.

With respect to claim 17, Merchant and Terasawa teach a bonding structure includes gold alloyed with a material having free energy lower than that of silicon oxide.

Thus, Merchant and Terasawa are shown to teach all the features of the claim with the exception of using the material selected from the group consisting of Ti, Al, Li, Mg and Ca.

However, Ohara teaches: bonding two semiconductor wafers (1 and 22) using a bonding structure including gold alloyed with a material selected from the group consisting of Ti and Al to obtain a good bondage. (col. 8, lines 18-67).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to bond the wafers of Merchant, in view of Terasawa using a boding structure including gold alloyed with a material selected from the group consisting of Ti and Al as taught by Ohara to obtain a good bondage and still be formed at a lower temperature.

Response to Arguments

6. Applicant's arguments with respect to claims 1, 10, 15 and 33 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 9:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Anh D. Mai
August 10, 2004